IDEC Chip Design Contest

An Ultra Low Static Power Level Shifter with Diode-Connected Cross-Coupled pFET and Stacked Split-Input Inverter

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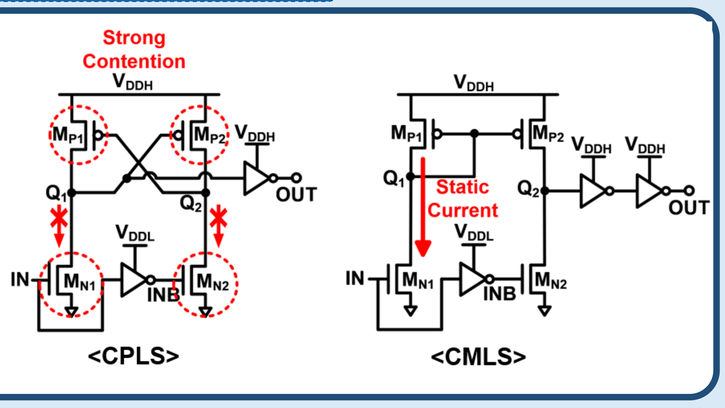
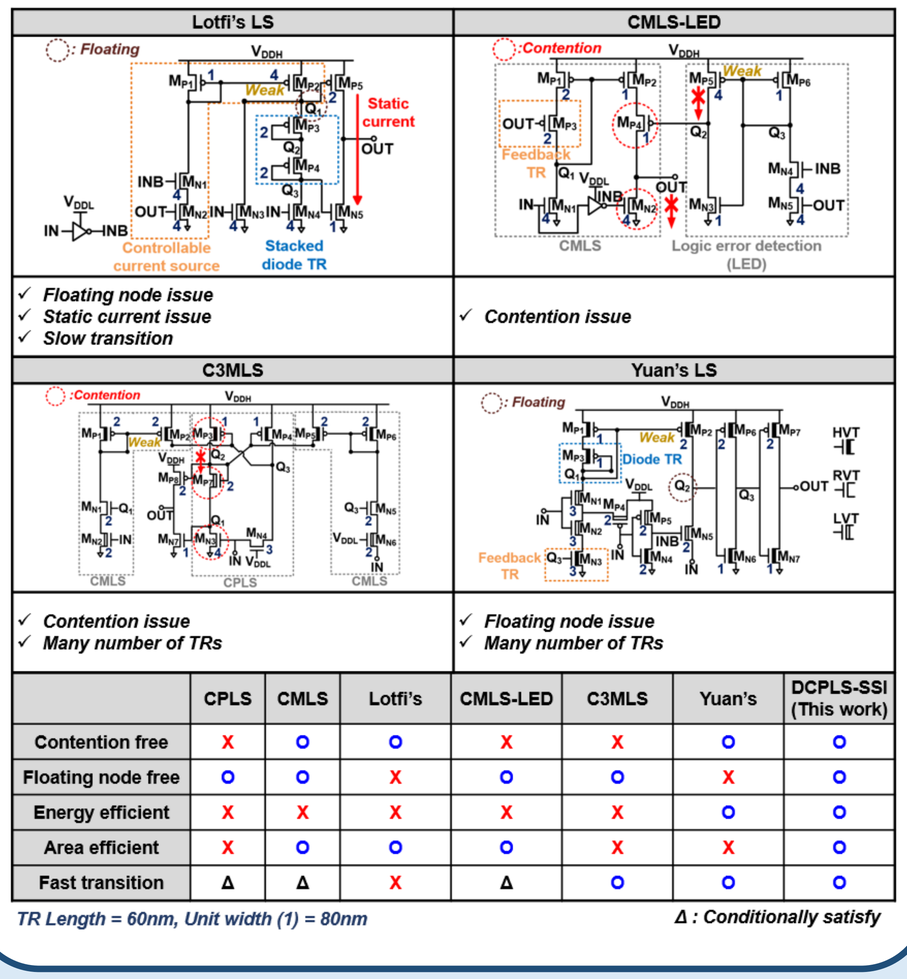
1. Introduction



- Level shifter (LS)는 SoC에서 multiple domain V_{DD} 사용 시, robust voltage conversion을 위해 필수적인 회로
- Conventional LS 구조로 Cross-coupled pFET LS (CPLS)와 Current mirror LS (CMLS)가 존재함
- CPLS는 current contention으로 인한 voltage conversion 제한 문제가 존재
- CMLS는 static current로 인해 energy 소모가 심한 한계점 존재

2. Limitations of previous LS

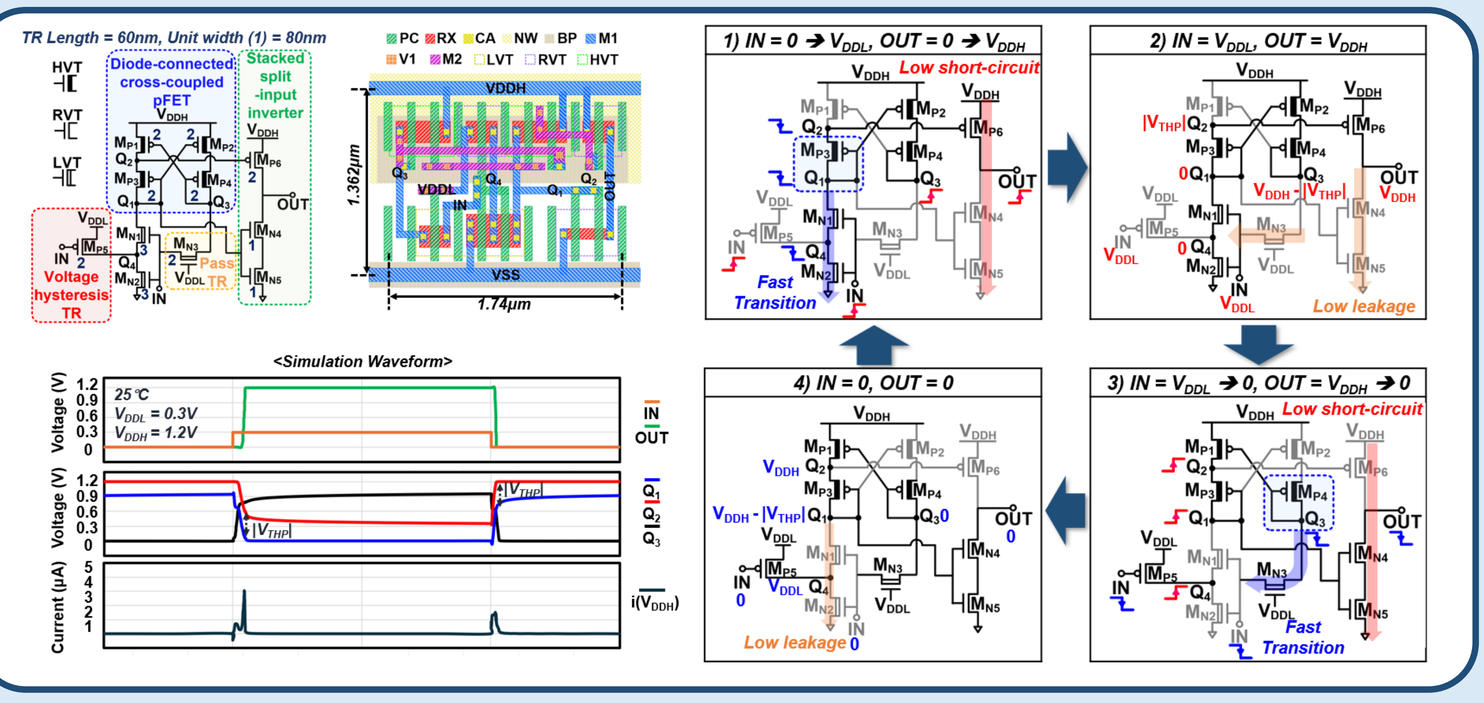


	CPLS	CMLS	Lotfi's	CMLS-LED	C3MLS	Yuan's	DCPLS-SSI (This work)
Contention free	X	O	O	X	X	O	O
Floating node free	O	O	X	O	O	X	O
Energy efficient	X	X	X	X	X	O	O
Area efficient	X	O	O	O	X	X	O
Fast transition	Δ	Δ	X	Δ	O	O	O

TR Length = 60nm, Unit width (1) = 80nm
Δ : Conditionally satisfy

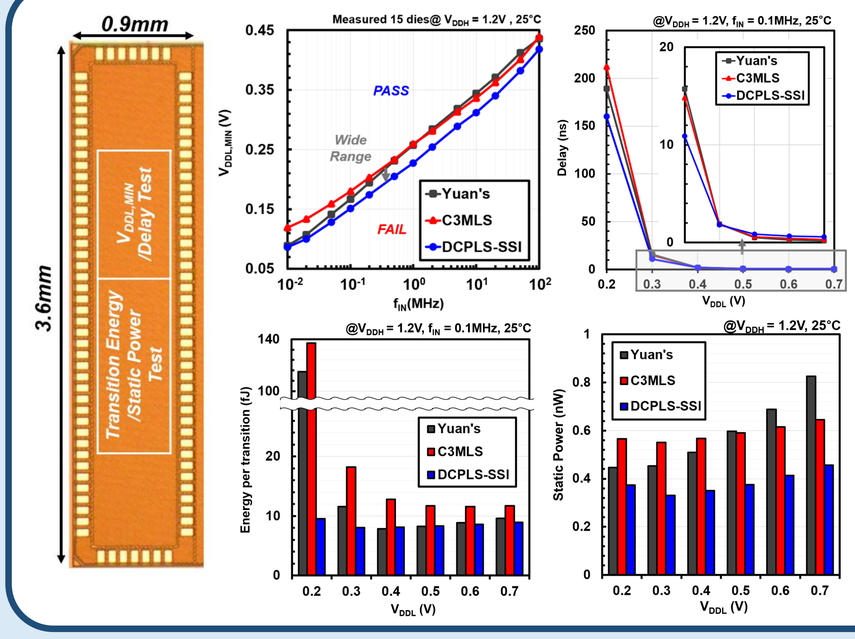
- Conventional LS 구조의 한계점을 해결하기 위해 여러 구조 들이 제안되었으나, 5가지 항목을 모두 만족시키지 못함
- CMLS-LED, C3MLS는 current contention으로 인해 voltage range 제약 및 performance 저하 발생
- Lotfi's LS 구조와 Yuan's LS 구조는 floating node 존재로 인해 performance 저하됨
- C3MLS와 Yuan's LS는 많은 TR 개수 사용으로 area overhead가 높음

3. Proposed DCPLS-SSI



- LS의 5가지 key characteristic을 만족하는 Diode-Connected Cross-Coupled pFET Level Shifter with Stacked Split-Input Inverter (DCPLS-SSI) 제안
- 제안 구조는 diode-connected cross-coupled pFET을 사용하여 current contention 문제 해결 및 floating node를 제거함
- Stacked-input inverter 사용을 통해 short-circuit current로 인한 energy 소모를 감소시킴
- Voltage hysteresis TR 사용으로 leakage current를 감소시켜 static power 소모를 줄임
- 11개의 적은 TR을 사용하여, 면적 소모 적음

4. Chip measurement



	Lotfi's		[c]CMLS-LED	[d]C3MLS		[d]Yuan's		[d]DCPLS-SSI
Journal/ Year	SSCL/ 2018		JSSC/ 2021	JSSC/ 2023		TCAS-II/ 2024		This work
Technology	40nm	28nm	28nm	55nm	28nm	55nm	28nm	**28nm**
Layout area (μm²)	8	2.85	3.08	9.98	3.78	7.94	3.62	**2.37**
V_{DDH}	1.1	1.2	1.2	1.2	1.2	1.2	1.2	**1.2**
V_{DDL_MIN}(V) @ f_{IN} (MHZ)	0.05 @0.01	0.28 @1	0.48 @1	0.196 @1	0.259 @1	0.13 @0.1	0.257 @1	**0.227 @1**
Delay (ns) @V_{DDL}(V)	80 @0.3	38.1 @0.3	Cannot operate V_{DDL} < 0.48V	20.08 @0.3	14.8 @0.3	13.86 @0.3	15.7 @0.3	**10.9 @0.3**
Energy per transition (fJ) @V_{DDL}(V)	18 @0.35	18.1 @0.3		18.11 @0.3	18.2 @0.3	22.71 @0.3	11.6 @0.3	**8.05 @0.3**
Static power (nW) @V_{DDL} (V)	0.6 @0.2	2.46 @0.3		0.12 @0.3	0.56 @0.3	0.035 @0.3	0.45 @0.3	**0.33 @0.3**
[a]Normalized EDP	-	7.86×		-	3.07×	-	2.08×	**1×**
[b]Normalized EDAP		9.45×			4.9×		3.17×	**1×**

All level shifter structures are re-implemented in 28nm CMOS technology
Gray column : Results of 10000 Monte Carlo post-layout simulation in 28nm CMOS technology @V_{DDH}=1.2V
[a]Normalized EDP : Energy-Delay-Product, normalized to DCPLS-SSI @V_{DDL}=0.3V and V_{DDH}=1.2V
[b]Normalized EDAP : Energy-Delay-Area-Product, normalized to DCPLS-SSI @V_{DDL}=0.3V and V_{DDH}=1.2V
[c]CMLS-LED reports only normalized values.
[d]Measured in 28nm CMOS technology

- 다양한 frequency, 전압 범위에서 LS test chip 검증을 진행함
- 제안 구조는 current contention과 floating node에 의한 performance 저하가 없음
- 기존 구조와 비교하여 wide-range voltage conversion이 가능함.
- Low supply voltage (V_{DDL})이 sub threshold region 에 근접한 영역에서 더욱 우수한 성능을 보임
- 기존 구조와 비교하여 0.3V to 1.2V voltage conversion에서 EDP, EDAP 성능이 매우 개선됨